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Design and Analysis of Fin FET based ALU for Nano-scale Technology

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Abstract: *An Arithmetic logic Unit (ALU) is treated as the supreme part of all microprocessors. It performs logical as well as arithmetic operations. It is declining in size and becoming more complex at the present time to bring out the expansion of a extra powerful but smaller design. Anyhow, there are a petty restricting motives that slows down the progress of smaller and extra tricky chip when CMOS is used. The principal limitations in scaling the bulk CMOS are short channel effects, sub-threshold leakage and gate-dielectric leakage. FinFET has an excellent control on short channel effects within the sub-micron regime as a result growing the probability to scale down the transistor. Due to this reason, the small size transistor can have a higher intrinsic gain and less off-state current in comparison with the majority counterpart. 8-bit ALU that performs basic logical, arithmetic, and shifting operations has been designed using FinFET structures.*
Keywords: *ALU, FinFET, IGFET, MOSFET, Sub-threshold leakages.*

I. Introduction

Fin-type FETs (FinFET) are trustable replacement for bulk CMOS on the nano-scale. FinFET can be double-gate devices. The 2 gates of these FETs can either be tied and handled together for better performance or independently handled for low leakage or decreased count of transistors. This offers a elevation to a appreciable design space.

The constant recession of MOSFETs with every new iteration of CMOS science has provide us with elevated circuit behavior and cost per function over a couple of many years. Nevertheless, ongoing transistor scaling may stand as a difficult goal to achieve in the 22 nm regime for the reason that of predominant fabric and approach science limits [1]. The predominant demands under this regime are the following two : (a) recession of current caused due to sub-threshold and gate leakages, and (b) variability reduction between device-to-device so as to expand yield [2]. Fin FETs were brought out as a trust-worthy replacement for out-crossing these challenges raised by the aid of non-ending scaling. Fabrication of Fin FET is suitable with those of conventional Mosfets, accordingly making viable highly rapid deployment of integrated manufacturing.

Fig. 1 suggests the outlook of a multi-fin FET where its outlook is quite different from the existing FETs. FinFET body is made of a thin silicon and its thickness denoted as TSi, covered all over through gate electrodes. The two gates as mentioned before, say front and back gates can be handled independently and this is successfully accomplished by taking off the gate on top portion of channel which is done by etching. Finfet's effective gate width is said to be 2*n*h, where the n is the fins count and h is fin's peak. Hence, transistors with more width and higher on-currents are acquired with the aid of employing fins in more number. The distance between two adjacent fins is considered as fin pitch. This pitch can be reduced during the layout part as the inclusions of multiple fins are done during the same [3].

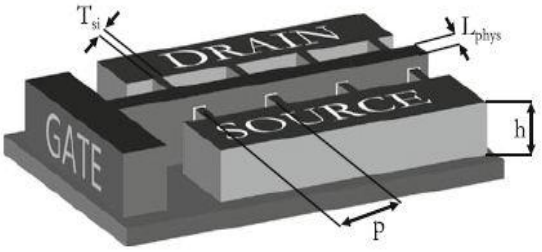

Figure1 Multi-fin Fin FET

a. Shorted-Gate(SG) and Independent-Gate(IG) Fin FET:

Fin FETs are available in many modes. In the mode of shorted-gate (SG) FinFET, the 2 gates(front and back) are held collectively, which leads to a 3-terminal device. This serves as an immediate substitute for the traditional MOS devices whereas in independent-gate mode (IG) FinFET, the top portion or area of the gate is taken off, giving method to two impartial or separate gates as depicted in Fig. 2. Considering the fact that the two

unbiased gates will also be handled separately, i.e one gate is used to alter the threshold of the other one. IG-mode Fin FET enables extra design choices.

b. Logic Design Using SG/IG-Mode Fin FET:

The efficiency and characteristics of power of FinFET logic gates utilizing transistors in quite a lot of connected configurations are explored subsequent. Generally 3 modes of Finfets are in use which are discussed here-SG-mode, in which both the gates of FinFET are held collectively; next is low-power (LP)-mode, where leakages in sub-threshold area is receded by connecting the back-gate bias to a voltage of reverse-bias[4] and IG-mode, where signals which are independent power the two gates.

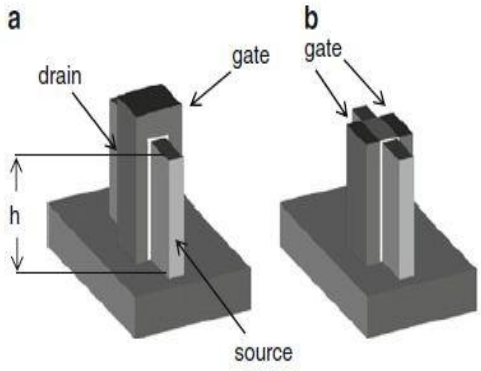

Figure 2 (a) SG-mode Fin FET; (b) IG-mode Fin FET

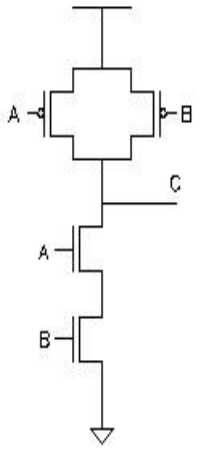

Figure 3: NAND Gate

The modes can be explained by considering NAND gate shown in Fig. 3 as an example. Let us matter the sizing of the FETs. All of the logic gates are designed in that way to possess the minimum viable size which are supported by FinFET models. The size of both pull-up as well as pull-down FETs are equal. 'β′ is used to indicate the ratio of pull-up transistor width and pull-down transistor width. To receiveβ, following cogitations are done-

1. Electron mobility outstrips gap mobility by 2x.
2. Fin FET's electrical width is figured out pertaining to the quantity of fins present in it. It is surmised that the transistors of more width are procured only by swelling the fin count and also it is deemed that the each and every fin's height is constant or stable.
3. Fin FETs deployed in the LP/IG modes may lead to the lessening of the drive strength by about 60 percent.

The NAND gate with Cmos technology can be transformed straightly to the one with SG-mode while still feasible to maintain the same size.

In the case of LP-mode implementation, the driving strength of each and every FinFET is diminished equitably. As a result, use of β=1 will be continued. As per the estimation, the gate used in LP-mode will have a delay equal to twice as compared to the gate used in SG-mode whereas the input capacitance is concerned, in LP-mode, it is best half of that present in SG-mode since the input signal drives only one gate of Finfet. Taking all input combos into consideration, the leakage power which is taken in average is decreased almost by 90% as the threshold voltage of these is also low.

Coming to the gate used in IG-mode, the rise and fall delays here are quite asymmetric. In this mode, only one gate is utilized for pull-up. In order to reap balance between the rise and fall delays, scaling up of the pull-ups is done. Anyways, by maintaining equal size for both pull-up and pull-down, in other words, keeping β=1, the input capacitance, area and gate output's diffusion capacitance can be saved. Accordingly, beneath unloaded stipulations, the NAND gate in IG-mode uses up lesser energy and area and its average is related or slightly finer than the gate in SG mode. Woefully, it is discovered that the power strengths of pull-up and pull-down are asymmetrical and this may cause great imbalance in rise and fall delays. If each transition via a gate is uncertain, the gate in IG-mode may be inharmonius. Hence, the SG mode is said to be more efficient compared to other modes according to the survey.

II. Proposed System

c. Implementation of 8 bit ALU

The design procedure of the ALU at transistor level uses the following steps.

1. By making use of the truth table the specifications compulsory for accomplishing the required functions are represented. This is done wherever required and can be done by other means as well.
2. Needed logic gates like AND, OR can be obtained by minimization or transformation methods.
3. The schematic diagram for the logic diagram is drawn in S-Edit of Tanner tool and then it is compiled to check for errors.
4. The design is implemented in transistor level.
5. The performance of ALU is obtained through H-Spice or TANNER EDA tools.

The design of 8-bit arithmetic & logic unit as shown in Fig. 4 performs one arithmetic, seven logical operations too. 8-bit ALU is designed by way of cascading 8 1-bit ALU blocks. A and B are inputs and S0,S1,S3 are the select lines of 8 down to 1 Mux implemented in each and every 1-bit ALU. The same signals hold good for 8-bit ALU too.

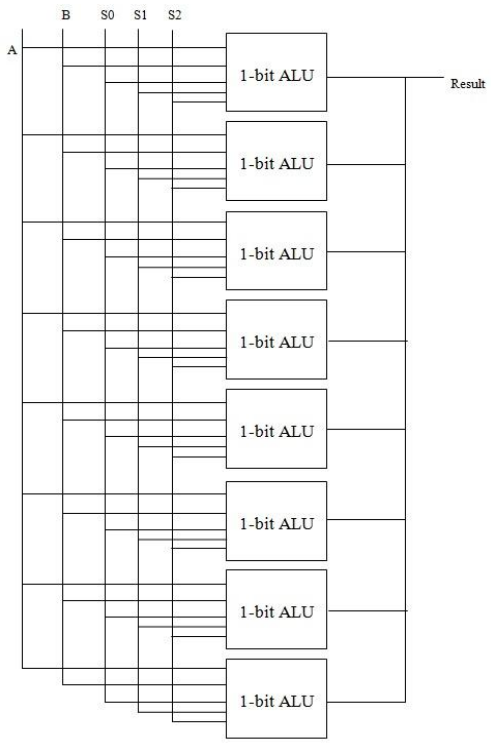

Figure 4: Block Diagram of Eight-bit ALU

Every 1-bit ALU consists of the following 4 components:
1. 2:1 multiplexer to come to a decision add/sub operation,
2. Circuit that does add and subtract,
3. Logical 8:1 multiplexer

To design the 8 bit ALU first we have to check the operation of the 1-bit ALU architecture as shown in Fig. 5. 1 bit ALU performs the logical and arithmetic operations on single bit input as per the select lines which define single operation at a time. The truth table of the single bit ALU is shown in table1. After successful simulation of the 1 bit ALU extend the 1 bit up to 8 bits by integrating the sixteen one bit ALU's as per the Fig 4. Before designing the one Bit ALU first we design all individual logic separately and cascade them with 8 to 1 MUX to form 1 bit ALU. Each bit of ALU operation requires 8 to 1 Multiplexer as mentioned above.

S2 S1 S0	Operations
000	ADD
001	AND
010	NAND
011	OR
100	XNOR
101	NOR
110	XOR
111	INVERT

Table 1. Truth Table for 1 bit ALU

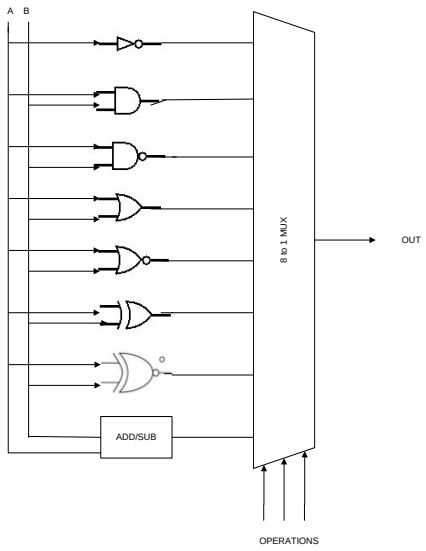

Figure 5: Single-bit ALU Architecture

Table 1 shows the truth table for 1-bit ALU. This shows the pattern of select lines S0, S1, S3 chosen for the operations to be performed by 1-bit ALU. These select lines are employed by MUX to guide it on the selection of operations.The operations performed by 1-bit ALU are designed in a Tanner tool in S-Edit. Later the code is written in T-Spice and required analysis is performed. Results for this analysis can later be seen in W-Edit.

III. Results

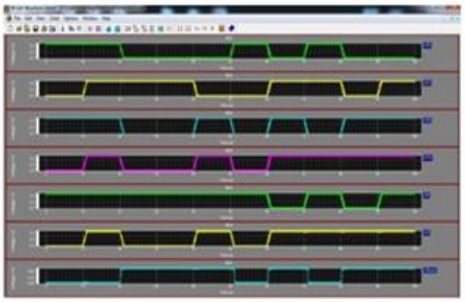

Figure 6: Simulation Result of a 1-Bit ALU

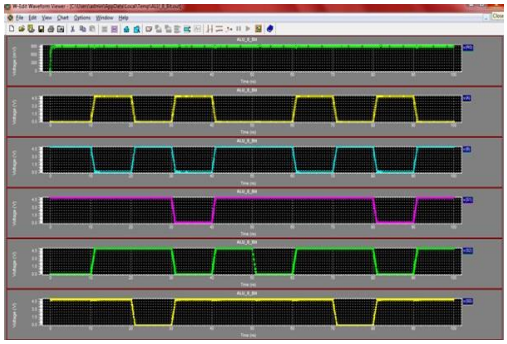

Figure 7: Simulation Result of an 8-Bit ALU

Fig 6 and Fig 7 shows the simulation results obtained for 1 and 8-bit ALU respectively. This is obtained by the transient analysis performed for the design and the code written in T-spice of tanner tool.

IV. Conclusion

The design of 8-bit ALU has been implemented by categorising it into different blocks as considered earlier. Low power and area efficiency is attained by independently optimising each and every block present in ALU. The design of 8-bit ALU here is employs DG-FinFET's 45nm technology. The area of ALU is optimized by lessening the count of transistors in the implementation of individual operation. This design can further be extended to 64 bits ALU as well. Here 22nm Finfets are used whereas the use of the technology below this is also acceptable. The main advantage of employing Finfets than Mosfets is that the fabulous recession in the leakage power as the motto of FinFETs is to defeat the short-channel effects completely.

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